



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Yeo, *et al.* Docket No.: TSM03-0421
Serial No.: 10/608,287 Art Unit: 2812
Filed: June 27, 2003 Examiner: TBD
For: Structure and Method for Forming the Gate Electrode in a Multiple-Gate Transistor

Certificate of Mailing via First Class Mail (37 C.F.R. § 1.8(a))

Date of Deposit: September 30, 2003

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Certificate of Mailing via First Class Mail (1 page)
Transmittal of Formal Drawings (1 page)
Drawing sheets (10 pages)
Information Disclosure Statement (1 page)
PTO/SB/08A (2 pages)
16 References Cited
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Respectfully submitted,

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Commissioner for Patents
P.O. Box 1450
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TRANSMITTAL OF FORMAL DRAWINGS

Submitted herewith are 10 sheets of formal drawings for the above-identified application.

Respectfully submitted,

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